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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/565,926
Filing Date: January 20, 2006
Appellant(s): VAN BERKEL ET AL.

Cornelis Hermanus Van Berkel, et al.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/27/2009 appealing from the Office action mailed 02/17/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

7,076,514	Erdogan et al.	7-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. Are claims 1-10 unpatentable under 35 U.S.C. 101 as being directed to non-statutory subject matter?

B. Are claims 1-11 unpatentable under 35 U.S.C. 102(c) as being anticipated by U.S. Patent No. 7,076,514 to Erdogan et al. (hereinafter referred to as "Erdogan")?

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-10 cite a device for composing a composite-code vector in accordance with a mathematical algorithm. However, device claims 1-10 merely disclose series units with mathematical operations for composing the composite-code vector without disclosing the hardware components of the device. Thus, these claiming component units

are reasonably considered as logical units and implemented by software modules.

Therefore, claims 1-10 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Erdogan et al. (U.S. 7,076,514).

Re claim 1, Erdogan et al. disclose in Figures 9-12 a device arranged to compose basic-code vectors into a composite-code vector (e.g. abstract, output of Figure 12, and col. 18 line 60 to col. 19 line 9), the device comprising: at least two weighted sum units (e.g. top and bottom portion of first set of weighted sum operation in Figure 12), each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors (e.g. col. 19 lines 17-35); an add unit (e.g. second adder in Figure 12), the add unit being arranged to sum the intermediate-code vectors into the composite-code vector (e.g. as summing the output of F1 and F2 in Figure 12); the weighted sum units being under the control of a first and a second configuration word (e.g. the words are the coefficients C11-C14 and C21-C24 as listed or described in col. 19 lines 17-35), wherein the first and the second configuration word are

deployed to configure the operations performed by the weighted sum units (e.g. as multiplied the input vector Dx with the coefficients Cx and summed up).

Re claim 2, Erdogan et al. further disclose in Figures 9-12 a pre-processing unit is coupled to at least one of the weighted sum units and to the add unit, the pre-processing unit being arranged to perform additional operations on the intermediate-code vector (e.g. by the F1 and F2 in Figure 12), the pre-processing unit being under the control of a third and a fourth configuration word (e.g. by the coefficients in col. 19 lines 36-62), wherein the third and the fourth configuration word are deployed to configure the additional operations on the intermediate-code vector (e.g. by additional filtering in col. 18 lines 60 to col. 19 line 9).

Re claim 3, Erdogan et al. further disclose in Figures 9-12 a post-processing unit is coupled to the add unit, the post-processing unit being arranged to perform additional operations on the composite-code vector (e.g. any operation after the second adder in Figure 12), the post-processing unit being under the control of a fifth configuration word, wherein the fifth configuration word is deployed to configure the additional operations on the composite-code vector (e.g. col. 19 lines 1-17).

Re claim 4, Erdogan et al. further disclose in Figures 9-12 the weighted sum units are arranged to calculate a bit-wise addition of at least two basic-code vectors (e.g. by the second adder in Figure 12).

Re claim 5, Erdogan et al. further disclose in Figures 9-12 the pre-processing unit is arranged to erase, repeat and reorder the elements of the intermediate-code vector (e.g. by the F1 or F2 in Figure 12).

Re claim 6, Erdogan et al. further disclose in Figures 9-12 the pre-processing unit is arranged to apply a mask on the intermediate-code vector (e.g. wherein the mask the set of coefficients in F1 and F2 in Figure 12 and col. 19 lines 35-62).

Re claim 7, Erdogan et al. further disclose in Figures 9-12 the post-processing unit is arranged to perform a conditional negation of the composite-code vector (e.g. col. 19 lines 1-17).

Re claim 8, Erdogan et al. further disclose in Figures 9-12 the weighted sum units and the add unit are arranged to be configured during a configuration stage of the operation of the device (e.g. Figure 12).

Re claim 9, Erdogan et al. further disclose in Figures 9-12 the pre-processing unit is arranged to be configured during a configuration stage of the operation of the device (e.g. Figure 12 and col. 18 line 60 to col. 19 line 19).

Re claim 10, Erdogan et al. further disclose in Figures 9-12 the post-processing unit is arranged to be configured during a configuration stage of the operation of the device (e.g. Figure 12).

Re claim 11, it is a method claim having similar limitations as cited in claim 1. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

(10) Response to Argument

A. Are claims 1-10 unpatentable under 35 U.S.C. 101 as being directed to non-statutory subject matter?

The applicant argues in pages 13-14 for claims 1-10 rejected under 35 U.S.C. 101 that claims 1-10 are statutory since it (1) falls within one of the four categories; (2) is not directed to judicial exception cause it generate a composite-code vector; and (3) does not impermissibly cover every substantial practical application. Further, the examiner erred in not entering the amendment to claim 1 prior the advisory since it does not raise new issues as the added limitation of a vector processor as seen in claim 11.

The examiner respectfully submits that not entering the amendment to claim 1 in the advisory seems proper because the amendment of claim 1 raise new issue rather than just the limitation "a vector processor" which is seen in claim 11. The amendment of claim 1 is not similar to claim 11 as alleged by the applicant but rather the amendment is directing to a new logical structure of the vector processor which comprising the weighted sum units and the added unit. These units structure within the vector processor is not seen in claim 11. Therefore, the amendment of claim 1 is considered as raising new matter which requires further consideration and/or search in order to make final and proper conclusion. The claims 1-10 are the device claims ({1} falls within one of the four categories), however these device claims do not provide physical structure for performing calculation steps in the claims. The claims comprise several software units for performing mathematical operations including weight, sum, and add the vector wherein the composite-code vector is just the mathematical result of the input vectors as called basic-code vectors. There is lacking of structure of the device in the claims in order to clearly place these claims as the device claims. Basically, the claims are directing to a preamble device comprising several mathematical units for weighting, summing and/or adding the input vector(s)

without efficiently tie or address physical structure of the device. Thus, claims 1-10 are reasonably considered as non-statutory claims.

B. Are claims 1-11 unpatentable under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,076,514 to Erdogan et al. (hereinafter referred to as "Erdogan")?

The applicant argues in pages 15-17 for claim 1 rejected under 35 U.S.C. 102(e) that the reference by Erdogan does not disclose "at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a "weighted sum of a plurality of the basic-code vectors" since provided Figure 12 with corresponding text portion does not disclose the weighted sum units as required in the claimed invention.

The examiner respectfully submits that the applicant does not address how the claiming language "weighted sum units" is different from the submitted reference by Erdogan, but rather argued the reference fails to disclose the language of "weighted sum units" as cited in claim 1. Generally, this specific limitation of claim 1 is seen clearly in Figure 12 of the cited reference by Erdogan et al. In either claim 1 or 11, the claim does not define or further explain the weighted sum units; intermediate- code vector; nor the basic-code vectors. The Examiner takes a broadest reasonable interpretation of these terms or phrases within the claims in light of the specification wherein the weighted sum units are the units that performs summing/adding all the weighted/scaled input data to generate the intermediate- code vector and the input data is the basic-code vectors. This reasonable interpretation is clearly seen in Figures 11-12 of the cited reference wherein the basic-code vectors are considered as the input data Dx vectors; the output of the second adder is considered as the intermediate-code vectors; and the core of weighted sum

units are seen in Figure 12 with the multiplication with coefficients (e.g. this is called scaling or weighting with factors/coefficients) and the adder for summing the input data vectors. In addition, the sum of the outputs of the filters are reasonable to be said as the weighted sum unit. For instant, the FIR filter which basically performs scaling/multiplication with coefficient/weighting and summing the all the scaling/weighting data to yield the result of filter which is exactly the same as the called "weighted sum unit" of the claimed invention. Even thought, the cited reference might not have or use the exact terminology or phrases as cited in the claims, but the contexts and functionalities of the claims are clearly seen in the cited reference as addressed above.

The applicant argues in pages 17-20 for claims rejected under 35 U.S.C. 102(e) that the first and second summers of Erdogan do not relate to standards and codes. Therefore, their outputs cannot be said to be an intermediate-code vector wherein the applicant intends the standards and codes to be within the Appellants' published application disclosures in pages 19-20.

The examiner respectfully submits that the claims do not specific or provide any definition of the basic-code vectors and composite-code vectors as seen in the specification as alleged by the applicant. In another words, the claims merely disclose the basic-code vector, intermediate-code vector and composite-code vector as the input vector, intermediate vector and the output vector of the mathematical operations. Nowhere within the claims would define any of those code vectors as vectors with specific definition relating to all coding techniques as disclosed in the specification. For examination purposes, the examiner reasonably interprets those the basic-code vector, intermediate-code vector and composite-code vector as merely the

input data vector, intermediate data vector and the output data vector which is clearly seen in Figures 11-12 wherein the intermediate data vector is the data vector of any intermediate operation of the mathematical operations. Further, Erdogan also discloses these data vectors are relating to the coding for transmission in columns 1-2 as described in the instant application.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Chat C. Do/

Primary Examiner, Art Unit 2193

October 19, 2009

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